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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,227	11/13/2003	Hung Y. Ng	END920030086US1	1174

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EXAMINER	
NOVACEK, CHRISTY L	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 12/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/713,227	NG ET AL.	
	Examiner	Art Unit	
	Christy L. Novacek	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 11-32* is/are pending in the application.

4a) Of the above claim(s) *22-31* is/are withdrawn from consideration.

5)☒ Claim(s) *13-21* is/are allowed.

6)☒ Claim(s) *1-4,6,8,9,11,12 and 32* is/are rejected.

7)☒ Claim(s) *5 and 7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed September 26, 2005.

Election/Restrictions

This application contains claims 22-31 drawn to an invention nonelected with traverse in the election filed April 27, 2005. A complete reply to the final rejection must include cancelation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Response to Amendment

The limitations added to claims 1 and 13 are sufficient to overcome the Lin et al. (US 6,743,669), Shin et al. (US 20020037611) and Sugiyama et al. (US 6,800,909) references. Therefore, the rejections of claims 1-3, 7, 10, 13, 16 and 17 as being anticipated by Lin et al., the rejections of claims 1-3, 8, 11-13, 17, 18, 20 and 21 as being anticipated by Shin et al. and the rejections of claims 1-3, 6, 9, 13, 14, 17 and 19 as being anticipated by Sugiyama et al. are hereby withdrawn.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-5 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krivokapic et al. (US 6,512,273, previously cited) in view of Yu et al. (US 5,747,373).

Regarding claim 1, Krivokapic discloses providing a substrate (2) having a gate stack (8/10) on the surface of the substrate, forming an etch resistant liner (18) over the gate stack,

forming a spacer (20) over the liner along sidewalls of the gate stack, removing the liner from regions of the substrate and gate stack not covered by the spacer, and leaving the liner in regions of the substrate and gate stack covered by the spacer (col. 4, ln. 38 – col. 5, ln. 40). Krivokapic discloses that the method of forming a semiconductor device "may then continue with standard CMOS processing including silicidation and metallization." (col. 5, ln. 37-40). But Krivokapic does not specifically disclose performing a preclean process to etch surfaces of the substrate not covered by the liner and then forming a conductive material in the regions of the substrate and gate stack not covered by the liner. Like Krivokapic, Yu discloses a process of forming a MOS transistor and siliciding regions of the transistor. Yu teaches that, prior to siliciding the substrate, it is necessary to preclean the substrate in order to remove native oxides (col. 4, ln. 34-38). At the time of the invention, it would have been obvious to one of ordinary skill in the art to preclean the substrate of Krivokapic before conducting the silicidation process as taught by Yu because the preclean is necessary to remove native oxides from the substrate surface. Yu also teaches that the silicidation involves forming a conductive material in the regions of the substrate and gate stack not covered by the liner (col. 4, ln. 45-52). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form conductive material in the regions of the substrate and gate stack not covered by the liner of Krivokapic because Krivokapic discloses using standard CMOS processing to silicide the transistor and Yu teaches that silicidation processing involves forming conductive material in the exposed regions of the substrate and gate stack.

Regarding claim 2, Krivokapic discloses, before forming the liner over the gate stack, providing a second gate stack (8/10) on the surface of the substrate (Fig. 2A).

Regarding claim 3, Krivokapic discloses forming the liner over the second gate stack, and forming the spacer over the liner along sidewalls of the second gate stack (Fig. 2B).

Regarding claim 4, Krivokapic discloses, before removing the liner from regions of the substrate and gate stack not covered by the spacer, and leaving the liner in regions of the substrate and gate stack covered by the spacer, depositing a photoresist layer over the liner and the spacer of the second gate stack to prevent removal of the liner from the second gate stack (Fig. 2C; col. 5, ln. 4-6).

Regarding claim 5, Krivokapic discloses, after removing the liner from regions of the substrate and gate stack not covered by the spacer, and leaving the liner in regions of the substrate and gate stack covered by the spacer, forming an insulative layer (38/34) on the surface of the substrate that covers the second gate stack before forming the conductive material (col. 5, ln. 19-39).

Regarding claim 32, Krivokapic discloses providing a substrate (2) having a gate stack (8/10) on the surface of the substrate, forming an etch resistant liner (18) over the gate stack, forming a spacer (20) over the liner along sidewalls of the gate stack, removing the liner from regions of the substrate and gate stack not covered by the spacer, and leaving the liner in regions of the substrate and gate stack covered by the spacer, wherein the remaining portions of the liner establish a region adjacent to a base of the gate stack (col. 4, ln. 38 – col. 5, ln. 40). Krivokapic discloses that the method of forming a semiconductor device "may then continue with standard CMOS processing including silicidation and metallization." (col. 5, ln. 37-40). But Krivokapic does not specifically disclose performing a preclean process to etch surfaces of the substrate not covered by the liner and then forming a conductive material in the regions of the substrate and

gate stack not covered by the liner. Like Krivokapic, Yu discloses a process of forming a MOS transistor and siliciding regions of the transistor. Yu teaches that, prior to siliciding the substrate, it is necessary to preclean the substrate in order to remove native oxides (col. 4, ln. 34-38). At the time of the invention, it would have been obvious to one of ordinary skill in the art to preclean the substrate of Krivokapic before conducting the silicidation process as taught by Yu because the preclean is necessary to remove native oxides from the substrate surface. Yu also teaches that the silicidation involves forming a conductive material in the regions of the substrate and gate stack not covered by the liner (col. 4, ln. 45-52). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form conductive material in the regions of the substrate and gate stack not covered by the liner of Krivokapic because Krivokapic discloses using standard CMOS processing to silicide the transistor and Yu teaches that silicidation processing involves forming conductive material in the exposed regions of the substrate and gate stack.

Claims 1, 8, 11 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rendon et al. (US 6,908,822) in view of Yu et al. (US 5,747,373).

Regarding claim 1, Rendon discloses providing a substrate (12) having a gate stack (18/16) on the surface of the substrate, forming an etch resistant liner (28) over the gate stack, forming a spacer (26) over the liner along sidewalls of the gate stack, removing the liner from regions of the substrate and gate stack not covered by the spacer, and leaving the liner in regions of the substrate and gate stack covered by the spacer (col. 2, ln. 53 – col. 6, ln. 41). Rendon discloses siliciding the substrate (col. 4, ln. 41-53). But Rendon does not specifically disclose performing a preclean process to etch surfaces of the substrate not covered by the liner and then

forming a conductive material in the regions of the substrate and gate stack not covered by the liner. Like Rendon, Yu discloses a process of forming a MOS transistor and siliciding regions of the transistor. Yu teaches that, prior to siliciding the substrate, it is necessary to preclean the substrate in order to remove native oxides (col. 4, ln. 34-38). At the time of the invention, it would have been obvious to one of ordinary skill in the art to preclean the substrate of Rendon before conducting the silicidation process as taught by Yu because the preclean is necessary to remove native oxides from the substrate surface. Yu also teaches that the silicidation involves forming a conductive material in the regions of the substrate and gate stack not covered by the liner (col. 4, ln. 45-52). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form conductive material in the regions of the substrate and gate stack not covered by the liner of Rendon because Rendon discloses siliciding the transistor and Yu teaches that silicidation processing involves forming conductive material in the exposed regions of the substrate and gate stack.

Regarding claims 8 and 11, Rendon discloses that the liner can be made of aluminum oxide or hafnium oxide (col. 3, ln. 52-58). These dielectrics inherently have a dielectric constant in the range of 7-150.

Regarding claim 32, Rendon discloses providing a substrate (12) having a gate stack (18/16) on the surface of the substrate, forming an etch resistant liner (28) over the gate stack, forming a spacer (26) over the liner along sidewalls of the gate stack, removing the liner from regions of the substrate and gate stack not covered by the spacer, and leaving the liner in regions of the substrate and gate stack covered by the spacer, wherein the remaining portions of the liner establish a region adjacent to a base of the gate stack (col. 2, ln. 53 – col. 6, ln. 41). Rendon

discloses siliciding the substrate (col. 4, ln. 41-53). But Rendon does not specifically disclose performing a preclean process to etch surfaces of the substrate not covered by the liner and then forming a conductive material in the regions of the substrate and gate stack not covered by the liner. Like Rendon, Yu discloses a process of forming a MOS transistor and siliciding regions of the transistor. Yu teaches that, prior to siliciding the substrate, it is necessary to preclean the substrate in order to remove native oxides (col. 4, ln. 34-38). At the time of the invention, it would have been obvious to one of ordinary skill in the art to preclean the substrate of Rendon before conducting the silicidation process as taught by Yu because the preclean is necessary to remove native oxides from the substrate surface. Yu also teaches that the silicidation involves forming a conductive material in the regions of the substrate and gate stack not covered by the liner (col. 4, ln. 45-52). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form conductive material in the regions of the substrate and gate stack not covered by the liner of Rendon because Rendon discloses siliciding the transistor and Yu teaches that silicidation processing involves forming conductive material in the exposed regions of the substrate and gate stack.

Claims 1-3, 6, 12 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeap et al. (US 6,753,242) in view of Yu et al. (US 5,747,373).

Regarding claim 1, Yeap discloses providing a substrate (62) having a gate stack (16/64) on the surface of the substrate, forming an etch resistant liner (86) over the gate stack, forming a spacer (88) over the liner along sidewalls of the gate stack, removing the liner from regions of the substrate and gate stack not covered by the spacer, and leaving the liner in regions of the substrate and gate stack covered by the spacer (col. 2, ln. 49 – col. 3, ln. 58). Yeap discloses

siliciding the substrate (col. 3, ln. 39-44). But Yeap does not specifically disclose performing a preclean process to etch surfaces of the substrate not covered by the liner and then forming a conductive material in the regions of the substrate and gate stack not covered by the liner. Like Yeap, Yu discloses a process of forming a MOS transistor and siliciding regions of the transistor. Yu teaches that, prior to siliciding the substrate, it is necessary to preclean the substrate in order to remove native oxides (col. 4, ln. 34-38). At the time of the invention, it would have been obvious to one of ordinary skill in the art to preclean the substrate of Yeap before conducting the silicidation process as taught by Yu because the preclean is necessary to remove native oxides from the substrate surface. Yu also teaches that the silicidation involves forming a conductive material in the regions of the substrate and gate stack not covered by the liner (col. 4, ln. 45-52). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form conductive material in the regions of the substrate and gate stack not covered by the liner of Yeap because Yeap discloses siliciding the transistor and Yu teaches that silicidation processing involves forming conductive material in the exposed regions of the substrate and gate stack.

Regarding claim 2, Yeap discloses, before forming the liner over the gate stack, providing a second gate stack on the surface of the substrate (Fig. 19-22).

Regarding claim 3, Yeap discloses forming the liner over the second gate stack, and forming the spacer over the liner along sidewalls of the second gate stack (Fig. 22).

Regarding claim 6, Yeap discloses forming a first spacer (122/124) along the sidewalls of the first and second gate stacks before forming the liner over the gate stacks (Fig. 19-22).

Regarding claim 12, Yeap discloses forming source and drain regions (90) within the substrate such that a location of the source and drain regions is determined by an end of the liner created by removing the liner from regions not covered by the spacer (Fig. 16; col. 3, ln. 34-37).

Regarding claim 32, Yeap discloses providing a substrate (62) having a gate stack (16/64) on the surface of the substrate, forming an etch resistant liner (86) over the gate stack, forming a spacer (88) over the liner along sidewalls of the gate stack, removing the liner from regions of the substrate and gate stack not covered by the spacer, and leaving the liner in regions of the substrate and gate stack covered by the spacer, wherein the remaining portions of the liner establish a region adjacent to a base of the gate stack (col. 2, ln. 49 – col. 3, ln. 58). Yeap discloses siliciding the substrate (col. 3, ln. 39-44). But Yeap does not specifically disclose performing a preclean process to etch surfaces of the substrate not covered by the liner and then forming a conductive material in the regions of the substrate and gate stack not covered by the liner. Like Yeap, Yu discloses a process of forming a MOS transistor and siliciding regions of the transistor. Yu teaches that, prior to siliciding the substrate, it is necessary to preclean the substrate in order to remove native oxides (col. 4, ln. 34-38). At the time of the invention, it would have been obvious to one of ordinary skill in the art to preclean the substrate of Yeap before conducting the silicidation process as taught by Yu because the preclean is necessary to remove native oxides from the substrate surface. Yu also teaches that the silicidation involves forming a conductive material in the regions of the substrate and gate stack not covered by the liner (col. 4, ln. 45-52). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form conductive material in the regions of the substrate and gate stack not covered by the liner of Yeap because Yeap discloses siliciding the transistor and Yu teaches

that silicidation processing involves forming conductive material in the exposed regions of the substrate and gate stack.

Claims 1, 9, 12 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (US 6,613,637) in view of Yu et al. (US 5,747,373).

Regarding claim 1, Lee discloses providing a substrate (201) having a gate stack (202/208) on the surface of the substrate, forming an etch resistant liner (218) over the gate stack, forming a spacer (219) over the liner along sidewalls of the gate stack, removing the liner from regions of the substrate and gate stack not covered by the spacer, and leaving the liner in regions of the substrate and gate stack covered by the spacer (Fig. 2D′-2E′; col. 6, ln. 11–29; col. 5, ln. 61 – col. 6, ln. 10). Lee discloses performing a preclean process to etch surfaces of the substrate not covered by the liner and siliciding the substrate (col. 5, ln. 64 – col. 6, ln. 10). But Lee does not specifically disclose forming a conductive material in the regions of the substrate and gate stack not covered by the liner. Like Lee, Yu discloses a process of forming a MOS transistor and siliciding regions of the transistor. Yu teaches that the silicidation involves forming a conductive material in the regions of the substrate and gate stack not covered by the liner (col. 4, ln. 45-52). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form conductive material in the regions of the substrate and gate stack not covered by the liner of Lee because Lee discloses siliciding the transistor and Yu teaches that silicidation processing involves forming conductive material in the exposed regions of the substrate and gate stack.

Regarding claim 9, Lee discloses that the liner is made of silicon carbide (col. 4, ln. 46-62).

Regarding claim 12, Lee discloses forming source and drain regions within the substrate such that a location of the source and drain regions is determined by an end of the liner created by removing the liner from regions not covered by the spacer (col. 5, ln. 61-64).

Regarding claim 32, Lee discloses providing a substrate (201) having a gate stack (202/208) on the surface of the substrate, forming an etch resistant liner (218) over the gate stack, forming a spacer (219) over the liner along sidewalls of the gate stack, removing the liner from regions of the substrate and gate stack not covered by the spacer, and leaving the liner in regions of the substrate and gate stack covered by the spacer, wherein the remaining portions of the liner establish a region adjacent to a base of the gate stack (Fig. 2D′-2E′; col. 6, ln. 11–29; col. 5, ln. 61 – col. 6, ln. 10). Lee discloses performing a preclean process to etch surfaces of the substrate not covered by the liner and siliciding the substrate (col. 5, ln. 64 – col. 6, ln. 10). But Lee does not specifically disclose forming a conductive material in the regions of the substrate and gate stack not covered by the liner. Like Lee, Yu discloses a process of forming a MOS transistor and siliciding regions of the transistor. Yu teaches that the silicidation involves forming a conductive material in the regions of the substrate and gate stack not covered by the liner (col. 4, ln. 45-52). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form conductive material in the regions of the substrate and gate stack not covered by the liner of Lee because Lee discloses siliciding the transistor and Yu teaches that silicidation processing involves forming conductive material in the exposed regions of the substrate and gate stack.

Response to Arguments

Applicant's arguments, filed September 26, 2005, with respect to the rejection(s) of claim(s) 1 and 13 have been fully considered and are persuasive. Therefore, these rejections have been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of the Krivokapic, Yu, Rendon, Yeap and Lee references.

Allowable Subject Matter

Claims 5 and 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 13-21 are allowed.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (571) 272-1839. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLN
December 5, 2005

ZANDRA V. SMITH
PRIMARY EXAMINER
12/7/05